REMARKS

Claims 1-17 are now pending in this application. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

In the Office Action dated April 10, 2007, Claims 1-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,076,060 (hereinafter "Bilchev") in view of U.S. Patent App. Pub. No. 2002/0083330 (hereinafter "Shiomi"). Applicants respectfully traverse these rejections at least the following reasons.

Claims 1-3, 9, 11, 13, and 15

With regard to Claim 1, the Examiner asserts that Bilchev discloses all limitations recited in Claim 1 except simulation means. Thus, the Examiner combined Bilchev with Shiomi alleging that Shiomi discloses a design/verification process as simulation means. More specifically, the Examiner asserts that the design/verification process of Shiomi can be used as the input and/or output devices of Bilchev.

Applicants respectfully submit that Shiomi fails to disclose **intermediate** data generated during a simulation by the simulation means. Although intermediate data generated by the simulation means may be temporarily stored in a storage means for being referred by the simulation means itself, the intermediate data is usually not accessible from the outside. In other words, the intermediate data generated during the simulation is not available as an output of the simulation means. Indeed, the design/verification system in Shiomi can output only verified results or circuit design data (please see Fig. 1 of Shiomi). Thus, Shiomi fails to disclose not

only that intermediate data presents, but also that intermediate data generated **during a simulation**, if presented, could be available as an output as the simulation means.

It is further submitted that the present invention was made in light of the problem where the intermediate data during a simulation may be accessed accidentally or on purpose breaking confidentiality (See page 2, line 25 – page 3, line 10 of the Specification). Such access does not usually occur because intermediate data is not output. However, when, in an unusual condition, the intermediate data is accessed by the third party, confidentiality of the circuit design will be breached. In order to solve this problem, the present invention employs "intermediate data encrypting means for encrypting intermediate data generated during a simulation by the simulation means."

Therefore, even assuming arguendo that the design/verification process of Shiomi operates as the input and/or output devices of Bilchev, the combination fails to disclose intermediate data encrypting means for encrypting intermediate data generated during a simulation by the simulation means.

In order to establish *prima facie* obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. ***In re Rokya***, 490 F. 2d 981, 180 USPQ 580 (CCPA 1974). At a minimum, the cited prior art does not disclose expressly or inherently the above recited limitation. Thus, Applicants respectfully request that the Examiner withdraw the rejection of Claim 1. Since Claims 2 and 3 depend from Claim 1, it is submitted that these claims are also allowable for the same reason as Claim 1.

With regard to Claims 9, 11, 13 and 15, the combination of Bilchev and Shiomi fails to disclose "intermediate data encrypting means for encrypting intermediate data generated during a simulation by the simulation means" or "an intermediate data encrypting step of encrypting

intermediate data generated during a simulation in the simulation step." Therefore, Applicants respectfully request that the Examiner withdraw the rejections of Claims 9, 11, 13 and 15 for at least the same reason as Claim 1.

Claims 4-8, 10, 12, 14, 16, and 17

With respect to Claim 4, the Examiner asserts that Bilchev discloses all limitations recited in Claim 1 except simulation means. Thus, the Examiner combines Bilchev with Shiomi alleging that Shiomi discloses a design/verification process as simulation means. More specifically, the Examiner asserts that Bilchev discloses different encryption techniques as a first and a second encryption technique recited in Claim 4.

Applicants respectfully submit that Bilchev fails to disclose a first and second encryption technique as recited by Claim 4. The Examiner asserts that Bilchev discloses three-input logic gates, gates using multiplexer, and/or gates using three-state buses as shown in Figs. 19-22 which can be used for a cipher unit 40 of Figs. 3-4 of Bilchev.

It is submitted that the Examiner misunderstood the circuit alternatives shown in Figs. 19-22 of Bilchev. In Bilchev, although several alternative circuit configurations shown in Fig. 19-22 may be used for a cipher unit 40, once one of them is selected for the system, the same circuit configuration is continuously used. In other words, during cipher operations, the same circuit configuration is used and the same encryption technique is used for the encryption and decryption in the cipher operations. Accordingly, even though Bilchev disclose reversible cipher units for encryption and decryption by changing the signal flow as shown in Figs. 3 and 4, the same encryption technique (the same circuit configuration) is used. Thus, Bilchev fails to disclose "supplied circuit information decrypting means for decrypting supplied circuit

information encrypted by a first encryption technique and stored circuit information encrypting means for encrypting, by a second encryption technique, the circuit information decrypted by the supplied circuit information decrypting means."

It is noted that the outputs of Figs. 19-22 are the same (B' and C'), which means the encrypted result is the same among the circuits. On the other hand, in the present invention, different encryption techniques are used for the encryption steps. In other words, the supplied circuit information encrypted by a first encryption technique and the circuit information encrypted by a second encryption technique are different from each other, which means the encrypted results by the first and the second encryption techniques are different.

One of the practical examples is explained as follows for illustrative purposes. The encryption section in the encryption apparatus shown in Fig. 3 of the present invention encrypts the circuit information by the first encryption technique and outputs the supplied circuit information. The supplied circuit information decrypting section 101 in the circuit operation simulating apparatus 100 shown in Figs. 1 and 3 decrypts the supplied circuit information by the first encryption technique. Though the decryption operation may be different from the encryption operation, each operation should correspond to each other as the same first encryption technique.

The stored circuit information encrypting section 102 shown in Fig. 1 encrypts the circuit information just decrypted by the supplied circuit information decrypting section 101 by the second encryption technique, and stores the circuit information encrypted to the storage section 103. If an encryption technique requiring short time for encryption and decryption is employed as the second encryption technique for example, the speed of simulation can be increased. Bilchev does not teach the stored circuit information encrypting section 102, nor the second encryption technique.

In order to establish *prima facie* obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. ***In re Rokya***, 490 F. 2d 981, 180 USPQ 580 (CCPA 1974). At a minimum, the cited prior art does not disclose expressly or inherently the above recited limitation. Thus, Applicants respectfully request that the Examiner withdraw the rejection of Claim 4. Since Claims 5-8 depend from Claim 4, it is submitted that these claims are also allowable for the same reason as Claim 4.

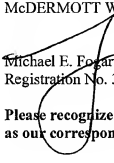
With regard to Claims 10, 12, 14, 16, and 17, the combination of Bilchev and Shiomi fails to disclose "supplied circuit information decrypting means for decrypting supplied circuit information encrypted by a first encryption technique and stored circuit information encrypting means for encrypting, by a second encryption technique, the circuit information decrypted by the supplied circuit information decrypting means, and for storing the encrypted circuit information in the storage means" or "a supplied circuit information decrypting step of decrypting supplied circuit information encrypted by a first encryption technique and a stored circuit information encrypting step of encrypting, by a second encryption technique, the circuit information decrypted in the supplied circuit information decrypting step and of storing the encrypted circuit information in storage means." Therefore, Applicants respectfully request that the Examiner withdraw the rejections of Claims 10, 12, 14, 16 and 17 at least the same reason as Claim 4.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:TS:lcb
Facsimile: 202.756.8087
Date: July 10, 2007